UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,658	01/22/2004	Dean Z. Tsang	TSA-001XX	5151

207 7590 10/13/2006

WEINGARTEN, SCHURGIN, GAGNEBIN & LEBOVICI LLP
TEN POST OFFICE SQUARE
BOSTON, MA 02109

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,658	TSANG, DEAN Z.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-35 is/are pending in the application.

4a) Of the above claim(s) 27-35 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 27-35, drawn to a method of making semiconductor device, classified in class 257, subclass 167.

II. Claims 1-26, drawn to a semiconductor device, classified in class 438, subclass 194.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process such as the source, drain, and gate contacts are formed simultaneously.

Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Thomas Hooever on 10/03/06 a provisional election was made with traverse to prosecute the invention of I, claims 1-26. Affirmation of this election must be made by applicant in replying to this Office action. Claims 27-35 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misewich et al. (US patent 6,365,913) in combination with Chu et al. (US publication 2004/0227154).

With respect to claims 1, 4, 5, Misewich et al. teach a transistor device comprising
(see claims 1-40 and associated figures):

a source;

a drain;

a gate;

a metal channel or channel layer;

Misewich et al. fail to teach the ranges for the thicknesses of the channel layer.

Chu et al. teach a MOS device in which the thickness of channel is between 1 .5 to 2.0 nm . See [00501].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use the range for the thickness of channel of Chu et al. in the device of Misewich et al. to achieve enhanced hole mobilities. See para [0050].

Further with respect to claim 1, it is submitted that the channel would inherently has carriers which are inherently controlled by the gate.

With respect to claim 3, Misewich et al. appear to fail to teach that substrate is made of silicon.

However, the use of silicon as substrate material is well-known in the art.

With respect to claim 2, Misewich et al. fail to teach that the channel is located between a gate insulator and an insulator.

However, the formation of a channel over a SOI substrate (including an insulator) and a gate insulator over the channel is well-known.

With respect to claims 6 and 7, Misewich et al. further teach that the transistor comprises of an enhancement or depletion mode device. See col. 1, lines 57-64.

With respect to claim 16, it is submitted that the channel would inherently have carriers which are inherently controlled by the gate.

With respect to claim 17, Misewich et al. further teach the source comprises a p-type metal and the drain comprises of a p-type metal and wherein the metal channel is a p-type metal (see fig. 1 and col. 6, lines 40-50). Further since Misewich et al. in combination with Chu et al. teach the claimed thickness for the metal channel, the carriers would inherently be controlled to form a p-channel depletion-mode device.

With respect to claim 18, Misewich et al. further teach the source comprises a n-type metal and the drain comprises of an p-type metal and wherein the metal channel is a p-type metal (see fig. 1 and col. 6, lines 40-50). Further since Misewich et al. in combination with Chu et al. teach the claimed device, an n-type inversion layer would inherently be formed on the p-type metal when a positive gate voltage is applied to form an n-channel enhancement mode device.

With respect to claim 19, Wisewich et al. further teach the device comprises of a CMOS device. See col. 6, lines 40-60.

With respect to claim 15, the formation of channel having plurality of layers is well-known.

With respect to claim 21, Wisewich et al. further teach the metal channel comprises of metal alloy. See col. 6, lines 40-50.

Claims 8, 9, 10, 11, 12, 13, 14, and 15 and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei et al. (US publication 2004/0169227) in combination with Misewich et al. (US patent 6,365,913), Chu et al. (US publication 2004/0227154), Song et al. (US patent 2004/0149579), and Ogura et al. (US publication 2002/0045319).

With respect to claim 8, Wei et al. teach a field effect transistor comprising (see figs. 1 and 2A-2B and associated text):

a channel 33 over an insulator 30B;

a source and a drain 52; and

a gate 36 and a gate insulator 34 over the channel.

Wei et al. fail to teach that the channel is made of n-type metal.

Misewich et al. teach channel made of metal to attain high density memory device, See claims 1-40 and col. 5, lines 60-62 and co. 6, lines 44-50.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use n-type metal as channel material to obtain above advantage.

Further with respect to claim 8, Wei et al. further teach the source and drain include p-type material. See col. [0025].

Further with respect to claim 8, it is submitted that the channel would inherently have carriers which are inherently controlled by the gate.

With respect to claim 9, Wei et al. further teach the insulator further comprises an insulating layer 30B over a substrate 30A, the channel being

positioned between the gate and the insulating layer and the gate insulator being positioned under the gate and over the channel.

With respect to claim 10, the use of silicon as substrate material is well-known.

With respect to claims 11 and 25, Wei et al. fail to teach the range for the thickness of the channel layer.

Chu et al. teach a MOS device in which the thickness of channel is between 1 .5 to 2.0 nm . See [0050].

Further with respect to claim 25, Since Wei et al. in combination with Chu et al. teach the claimed thickness of the channel layer, it is inherently greater than the thickness of the p-type inversion layer.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use the range for the thickness of channel of Chu et al. in the device of Wei et al. to achieve enhanced hole mobilities. See [0050].

With respect to claim 12, Wei et al. further teach the device comprises of a CMOS device. See [0007] .

With respect to claim 13, Wei et al. further teach an encapsulation layer 21. See fig. 1.

With respect to claim 14, Wei et al. fail to teach the range for the width of the channel.

Song et al. teach a channel having width of less than 500 nm. See claim 4.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use the range for width of the channel of Song et al. in the device of Wei et al. to achieve the benefit of controlling current flow through the channel by controlling the voltage applied across the channel. See [0005].

Further with respect to claim 14, Wei et al. fail to teach the range of the length of the channel.

Ogura et al. teach a channel having a length of 40 nm to reduce voltage and increase speed. See [0024].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use the length of the channel of Ogura et al. in the device of Wei et al. to achieve above advantage.

With respect to claim 15, the formation of channel having plurality of layers is well-known.

With respect to claim 24, Wisewich et al. further teach the metal channel comprises of metal alloy. See col. 6, lines 40-50.

With respect to claims 22, 23, and 26, since Wei et al. in combination with Misewich et al., Song et al, and Ogura et al. teach the claimed device, a p-type inversion layer would inherently be formed on a side of the n-type metal when a negative gate voltage is applied to form an p-channel enhancement mode device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

LP